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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,671	07/28/2004	Chih-Wei Hung	13085-US-PA	4670

31561 7590 08/24/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
KRAIG, WILLIAM F	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,671	HUNG ET AL.	
	Examiner	Art Unit	
	William Kraig	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *1* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/28/2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/28/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 132, defined as a "memory cell row" on line 9 of paragraph 36 of the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: The sentence beginning on line 1 of paragraph 11 of the specification is unclear. Examiner recommends replacing "are serial" with --being serially--.

The disclosure is objected to because of the following informalities: The sentence beginning on line 5 of paragraph 37 of the specification is unclear. Examiner recommends replacing "is" with --are--.

Appropriate correction is required.

Claim Objections

3. Claim 1 objected to because of the following informalities: Examiner believes there is an error on line 3 of the claim. After comparing the claim language with the content of the specification, Examiner recommends that line 3 should read --a plurality of gate structures, disposed on the substrate, wherein each *gate*--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2 and 7 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 2, claim 1 defines "gate structure" as not including the "spacers" (i.e. the spacers are "disposed ***between*** the gate structures and the select gate structures). Claim 1 thus implies that the "gate structures" and the "spacers" are distinctly separate objects. Therefore, regarding claim 2, the select

gate structures cannot possibly completely fill the space between the gate structures (as claimed) because claim 1 has already stated that aforementioned "spacers" exist in this space. For purposes of this office action, the Examiner will treat claim 2 as if the "spacers" of claim 1 are a part of the "gate structures", as seen in Fig. 2B. Examiner recommends that claim 2 should read --The non-volatile memory structure of claim 1, wherein said spacers are formed adjacent to and on both sides of each gate structure, wherein there is a space between said spacers not occupied by said gate structures, wherein each of the select gate structures completely fills said space between said spacers--.

Regarding claim 7, the source and drain regions as defined in the claims are not defined as disclosed in the drawings, nor as would be understood to be functional in the art. The claims define the source and drain regions as both being on the same side of the gate structure. Fig 2C discloses the source and drain regions as being on opposite sides of the gate structure. It is also generally understood in the art that the drain and source regions are to be disposed on opposite sides of the gate structure in order for the device to function as intended. For purposes of this office action, the Examiner will treat claim 7 as if the source and drain regions are on opposite sides of the gate structures as disclosed in Fig. 2C. Examiner also recommends that "a source region, disposed in the substrate on one side of the gate structure corresponding to the select gate" in claim 7 be replaced with --a source region, disposed in the substrate on one side of the gate structure opposite the select gate--.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 and 8-10 rejected under 35 U.S.C. 102(e) as being anticipated by Hsieh (U.S. Patent # 6645813).

Regarding claim 1, Fig. 2h of Hsieh discloses a non-volatile memory structure, comprising:

a substrate(100);

a plurality of gate structures(multiple layered structures built on top of oxide layers 110) disposed on the substrate(100), wherein each gate structure(multiple layered structures built on top of oxide layers 110) comprises, from the substrate(100), at least a bottom dielectric layer(bottom oxide layer of 130(Hsieh, Col. 7, Lines 14-20)), a charge-trapping layer(Nitride layer of 130(Hsieh, Col. 7, Lines 14-20)) , an upper dielectric layer(upper oxide layer of 130(Hsieh, Col. 7, Lines 14-20)), a control gate(140) and a cap layer(150) (Hsieh, Col. 7, Lines 34-37).

a plurality of select gate structures(210 and 220(divided as described on Lines 26-40, Column 8 of Hsieh)), wherein each of the select gate structures(210 and 220(divided as described on Lines 26-40, Column 8 of Hsieh)) is disposed on one side of each gate structure(multiple layered structures built on top of oxide layers 110) respectively such that the gate structures(multiple layered structures built on top of oxide layers 110) are serially connected together to form a memory cell row(the multi-bit split-gate flash memory cell described by Hsieh in Col. 8, Lines 36-52 and shown in Fig. 5f), wherein each select gate structure(210 and 220(divided as described on Lines 26-40, Column 8 of Hsieh)) comprises, from the substrate(100), at least a select gate dielectric layer(210) and a select gate(220(divided as described on Lines 26-40, Column 8 of Hsieh));

a plurality of spacers(170), disposed between the gate structures(multiple layered structures built on top of oxide layers 110) and the select gate structures(210 and 220(divided as described on Lines 26-40, Column 8 of Hsieh)); and

a source/drain region(107), disposed in the substrate(100) on each side of the memory cell row(the multi-bit split-gate flash memory cell described by Hsieh in Col. 8, Lines 36-52 and shown in Fig. 5f).

Regarding claim 2, Hsieh discloses the non-volatile memory structure of claim 1, wherein said spacers(170) are formed adjacent to and on both sides of each gate structure(multiple layered structures built on top of oxide layers 110)(Fig. 5f), wherein there are spaces(Fig. 5e, (125)) between said

spacers(170) not occupied by said gate structures(multiple layered structures built on top of oxide layers 110), wherein each of the select gate structures(210 and 220(divided as described on Lines 26-40, Column 8 of Hsieh)) completely fills said spaces(Fig. 5e, (125)) between said spacers(170).

Regarding claim 3, Hsieh discloses the non-volatile memory structure of claim 1, wherein material constituting the charge-trapping layer comprises silicon nitride. (Hsieh, Col. 7, Lines 14-20)

Regarding claim 4, Hsieh discloses the non-volatile memory structure of claim 1, wherein material constituting the bottom dielectric layer(bottom oxide layer of 130(Hsieh, Col. 7, Lines 14-20)) and the upper dielectric layer(upper oxide layer of 130(Hsieh, Col. 7, Lines 14-20)) comprises silicon oxide. (Hsieh, Col. 7, Lines 14-20)

Regarding claim 5, Hsieh discloses the non-volatile memory structure of claim 1, wherein material constituting the control gate(140) and the select gate(220(divided as described on Lines 26-40, Column 8 of Hsieh)) comprises polysilicon. (Hsieh, Col. 7, Lines 22-24)(Hsieh, Col. 8, Lines 26-40)

Regarding claim 6, Hsieh discloses the semiconductor device of claim 1 wherein the select gate dielectric layer has a thickness between about 160 Angstroms and 170 Angstroms. (Hsieh, Col. 8, Lines 20-26)

Regarding claim 8, Hsieh discloses the non-volatile memory structure of claim 1, wherein material constituting the charge-trapping (memory) layer comprises silicon nitride. (Hsieh, Col. 7, Lines 14-20)

Regarding claim 9, Hsieh discloses the non-volatile memory structure of claim 1, wherein material constituting the bottom dielectric layer(bottom oxide layer of 130(Hsieh, Col. 7, Lines 14-20)) comprises silicon oxide. (Hsieh, Col. 7, Lines 14-20)

Regarding claim 10, Hsieh discloses the non-volatile memory structure of claim 1, wherein material constituting the upper dielectric layer(upper oxide layer of 130(Hsieh, Col. 7, Lines 14-20)) comprises silicon oxide. (Hsieh, Col. 7, Lines 14-20)

6. Claim 7 rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. (U.S. Patent # 5969383).

Regarding claim 7, Fig. 1 of Chang et al. discloses a non-volatile memory structure, comprising:

a gate structure(23, 24, 28, 32, 34) having at least a bottom dielectric layer(23), a charge trapping layer(24), an upper dielectric layer(28), a control gate(32) and a cap layer(34) over a substrate(11);

a select gate(16), disposed on one side of the gate structure(23, 24, 28, 32, 34);

a spacer(23, along sidewall of select gate(16)), disposed between the gate structure(23, 24, 28, 32, 34) and the select gate(16);

a select gate dielectric layer(14), disposed between the select gate(16) and the substrate(11);

a source region(36), disposed in the substrate(11) on one side of the gate structure(23. 24, 28, 32, 34) opposite from the select gate(16); and

a drain region(22), disposed in the substrate(11) adjacent to the select gate(16).

Double Patenting

7. Applicant is advised that should claim 3 be found allowable, claim 8 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-0237. The examiner can normally be reached on Mon-Fri 8:00-4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFK

GEORGE ECKERT
PRIMARY EXAMINER